UTO-NBL-52A

Datasheet

2018

Version 01.6

Beyond the technology

Utovertek

VERSION HISTORY

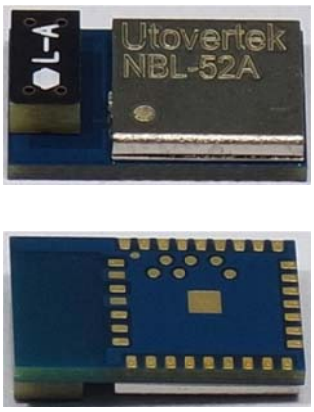
REVISION	AMENDMENT	DATE	
01.1	Initial version		
01.2	Minor change		
01.3	Dimension Change		
01.4	Dimension change		
01.6	BT SIG		

DESCRIPTION

UTO-NBL-52A is a built-in Antenna Bluetooth Low Energy Module. UTO-NBL-52A integrates all features of Bluetooth radio, software stack, GATT based profiles, antenna and host end user applications, which means no external micro controller. It provides a Bluetooth Low Energy fully compliant system for a data communication. At +4 dBm TX Power and -93dBm RX Sensitivity UTO-NBL-52A has best RF performance.

APPLICATION

- Commercial
- Sports and fitness
- Healthcare
- Medical sensors
- Home entertainment
- Mobile accessories
- Watch
- Human interface devices



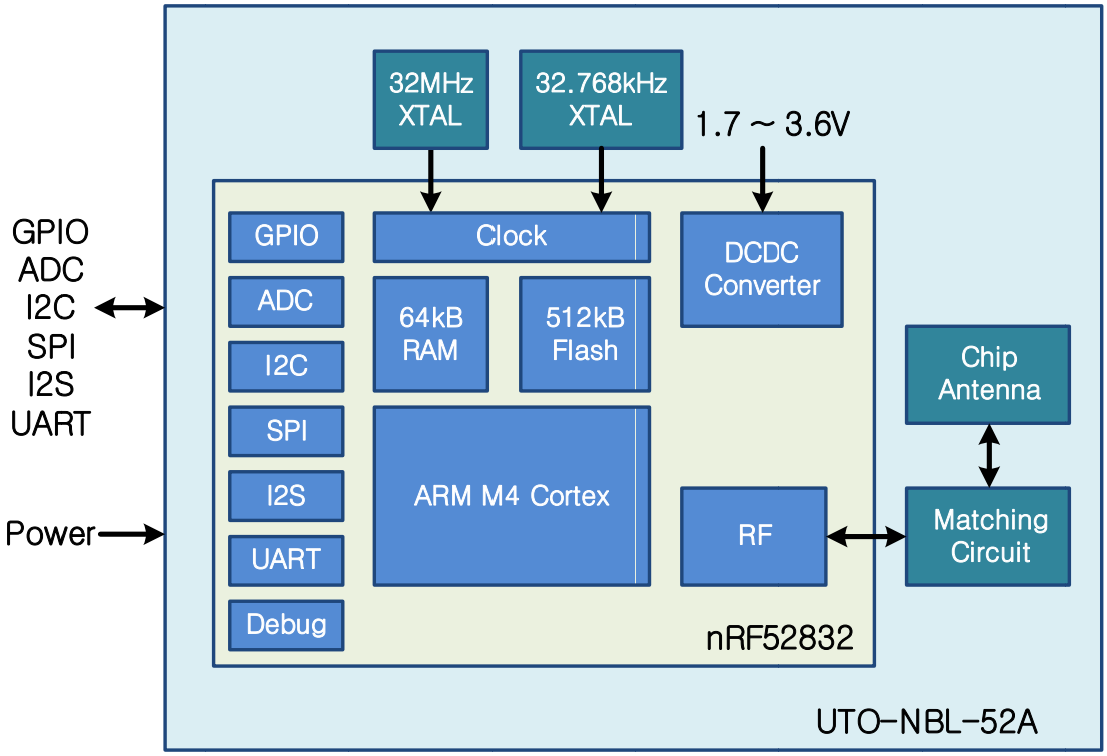
<Figure 1. UTO-NBL-52A >

FEATURE

- Bluetooth v5.0 Single Mode Compliant
- Integrated Bluetooth Smart Stack
  . GAP, GATT, L2CAP and SMP
  . Bluetooth Smart profiles
- RF Performance
  . Transmit power : +4 dBm (-20 dBm ~ +4 dBm)
  . Receiver sensitivity : -96 dBm
- Low Power Consumption
  . Transmit : 7.5 mA peak
  . Receiver : 12.9 mA peak
  . Sleep mode : 0.5 uA
- Peripheral Interfaces
  . UART/SPI(Master/Slave)/I2C
  . GPIO
  . 12-bit ADC
  . I2S and PDM
  . Timer
  . Temperature Sensor
- Power supply : 1.7 ~ 3.6 V
- Dimension : 5.9 x8.9 x 1.9 mm (W x L x H)

1. Block Diagram

UTO-NBL-52A's block diagram is illustrated in Figure 2 below.



<Figure 2. Simplified block diagram of UTO-NBL-52A>

CPU and Memory

The Main core is **ARM Cortex-M4**. The processor implements several features that enable energy-efficient arithmetic and high-performance signal processing including "digital signal processing", "Single-cycle multiply and accumulate instructions", "hardware divide", "8 and 16-bit single instruction multiple data instructions" and "Single-precision floating-point unit"

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the Nested Vectored Interrupt Controller (NVIC).

The floating point unit (FPU) may generate exceptions when used due to e.g. overflow or underflow. These exceptions will trigger the FPU interrupt.

The **64-KB SRAM** of 1024 byte page size and **512-KB flash** of 8-KB block size memory are provided.

Power management

UTO-NBL-52A supports two different power supply alternatives of Internal LDO mode and Low voltage mode. In **internal LDO mode**, the system power is generated directly from the supply voltage VDD. In **low voltage mode**, the system power is supplied by 1.8V.

The module's power management features are System OFF mode and System ON mode. In **system OFF mode**, the module is in deepest power saving mode. The system's core functionality is powered down and all ongoing tasks are terminated.

In **system ON mode**, the module is fully operational and CPU and selected peripherals can be brought into a state where they are functional and more or less responsive depending on the sub-power mode selected by Low power or Constant latency.

Clock management

The module has a 32 MHz main crystal oscillator and 32.768 kHz RTC crystal oscillator.

Peripherals

The **general GPIO** is organized as one port with up to 30 I/Os enabling access and control of up to 30 pins through one port. Each GPIO can be accessed individually with the following user configurable features.

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system. The maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- All pins can be individually configured to carry serial interface or quadrature demodulator signals.

The **transceiver** receives and transmits data directly to and from system memory for flexible and efficient packet data management. The module's transceiver has the following features.

- General modulation features
  - . GFSK modulation
  - . Data whitening
  - . On-air data rates (250 kbps/1 Mbps/2 Mbps)
- Transmitter with programmable output power of +4 dBm to -20 dBm, in 4 dB step
- RSSI function (1 dB resolution)
- Receiver with integrated channel filters achieving maximum sensitivity

- Baseband controller

  . EasyDMA RX and TX packet transfer directly to and from RAM

  . Dynamic payload length

  . On-the-fly packet assembly/disassembly and AES CCM payload encryption

  . 8 bit, 16 bit and 24 bit CRC check

The **timer** runs on the high-frequency clock source (HFCLK) and includes a four-bit (1/2X) prescaler that can divide the timer input clock from the HFCLK controller. Clock source selection between PCLK16M and PCLK1M is automatic according to TIMER base frequency set by the prescaler. The TIMER base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to trigger a task of any other system peripheral of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

The **temperature sensor** measures die temperature over the temperature range of the device with 0.25 degree resolution.

The **SPI** is implemented with EasyDMA support for ultra low power serial communication from an external SPI master. EasyDMA in conjunction with hardware-based semaphore mechanisms removes all real-time requirements associated with controlling the SPI slave from a low priority CPU execution context.

The **TWI** slave with EasyDMA (TWIS) is compatible with I2C operating at 100 kHz and 400 kHz. The TWI transmitter and receiver implement EasyDMA.

The Universal asynchronous receiver/transmitter with EasyDMA (**UART**) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps, and EasyDMA data transfer from/to RAM.

The **ADC** supports up to eight external analog input channels, depending on package variant. It can be operated in a one-shot mode with sampling under software control, or a continuous conversion mode with a programmable sampling rate. The analog inputs can be configured as eight single-ended inputs, four differential inputs or a combination of these. Each channel can be configured to select AIN0 to AIN7 pins, or the VDD pin. Channels can be sampled individually in one-shot or continuous sampling modes, or, using scan mode, multiple channels can be sampled in sequence. Channels can also be oversampled to improve noise performance.

The **I2S** (Inter-IC Sound) module, supports the original two-channel I2S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention. The I2S peripheral has the following main features :

- Master and Slave mode
- Simultaneous bi-directional (TX and RX) audio streaming
- Original I2S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- Low-jitter Master Clock generator
- Various sample rates

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Rating	Min	Max	Unit
Storage Temperature	-40	+120	Degree
VDD, VDD_RF	-0.3	3.9	V
Other Terminal Voltages	-0.3	VDD+0.3	V

<Table 1 : Absolutes Maximum Ratings>

2.2 Recommended Operating Conditions

Rating	Min	Max	Unit
Operating Temperature	-40	+85	Degree
VDD, VDD_RF*	1.7	3.6	V

<Table 2 : Recommended Operating conditions>

*) normal supply voltage is 3.0 ~ 3.3V

2.3 Current consumption

Power mode	Condition	Min	Typ	Max	Unit
Transmit (DCDC, 3V)	Pout = +4 dBm		7.5		mA
	Pout = 0 dBm		5.3		mA
Receive (DCDC, 3V)	At 1 Mbps		11.7		mA
	At 2 Mbps		12.9		mA

<Table 3 : Current consumption>

2.4 RF Characteristics

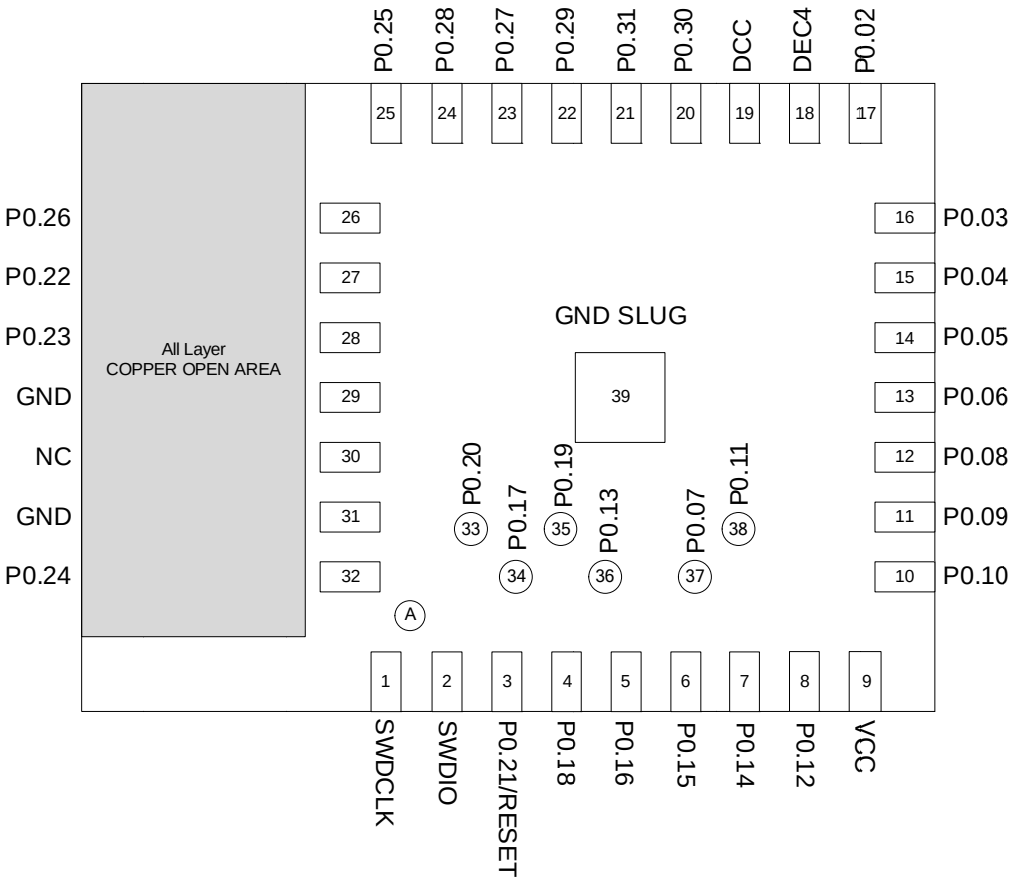
Rating	Min	Typ	Max	Unit
Operating frequencies	2360		2500	MHz
TX Maximum output power		4		dBm
TX RF power control range	20	24		dB
TX RF power accuracy			+/-4	dB
TX 1st Adjacent Channel Transmit Power (2 Mbps)		-25		dBc
TX 2nd Adjacent Channel Transmit Power (2 Mbps)		-50		dBc
TX 1st Adjacent Channel Transmit Power (1 Mbps)		-25		dBc
TX 2nd Adjacent Channel Transmit Power (1 Mbps)		-50		dBc
RX maximum received signal strength at < 0.1% PER		0		dBm
RX Sensitivity (0.1% BER) at 2 Mbps		-89		dBm
RX Sensitivity (0.1% BER) at 1 Mbps		-93		dBm
RX RSSI accuracy (-90 dBm to -20 dBm)		+/-2		dB
RX RSSI resolution		1		dB
RX RSSI sample period		8		us

<Table 4 : RF Characteristics>

3. Pin Description

UTO-NBL-52A's PIN descriptions are summarized in Figure 3 and Table 5 below.

UNIT : mm



A : No1 Mark.(0.3Ø GND)

- Top View (Bottom pad)

<Figure 3. PIN descriptions>

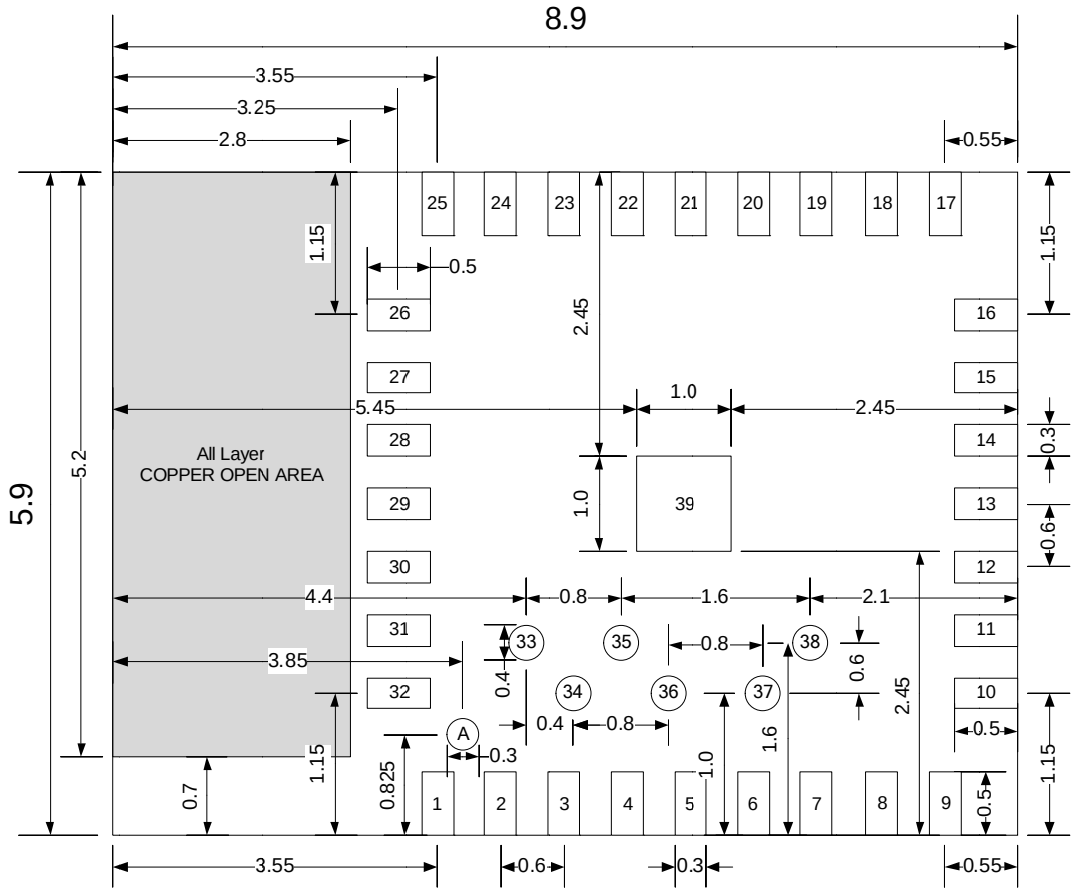
Num.	PIN Name	Type	Description
1	SWDCLK	DEBUG	Debug/Program
2	SWDIO	DEBUG	Debug/Program
3	P0.21/RESET	I/O	RESET(default)/Configurable I/O
4	P0.18	I/O	Configurable I/O
5	P0.16	I/O	Configurable I/O
6	P0.15	I/O	Configurable I/O
7	P0.14	I/O	Configurable I/O
8	P0.12	I/O	Configurable I/O
9	VCC	Supply Voltage	Power supply
10	P0.10	I/O	Configurable I/O
11	P0.09	I/O	Configurable I/O
12	P0.08	I/O	Configurable I/O
13	P0.06	I/O	Configurable I/O
14	P0.05	I/O	Configurable I/O
15	P0.04	I/O	Configurable I/O
16	P0.03	I/O	Configurable I/O
17	P0.02	I/O	Configurable I/O
18	DEC4	Supply Voltage	1.3V Regulator supply decoupling input from DC/DC Converter. Output from 1.3V LDO
19	DCC	Power out	DC/DC output voltage to external LC filter
20	P0.30	I/O	Configurable I/O
21	P0.31	I/O	Configurable I/O
22	P0.29	I/O	Configurable I/O
23	P0.27	I/O	Configurable I/O
24	P0.28	I/O	Configurable I/O
25	P0.25	I/O	Configurable I/O
26	P0.26	I/O	Configurable I/O
27	P0.22	I/O	Configurable I/O
28	P0.23	I/O	Configurable I/O
29	GND	GND	Ground
30	NC	NC	NC
31	GND	GND	Ground
32	P0.24	I/O	Configurable I/O
33	P0.20	I/O	Configurable I/O
34	P0.17	I/O	Configurable I/O

35	P0.19	I/O	Configurable I/O
36	P0.13	I/O	Configurable I/O
37	P0.07	I/O	Configurable I/O
38	P0.11	I/O	Configurable I/O
39	GND SLUG	GND	Ground PAD

<Table 5 : PIN descriptions>

4. Physical Dimensions

UNIT : mm



A : No1 Mark.(0.3Ø GND)

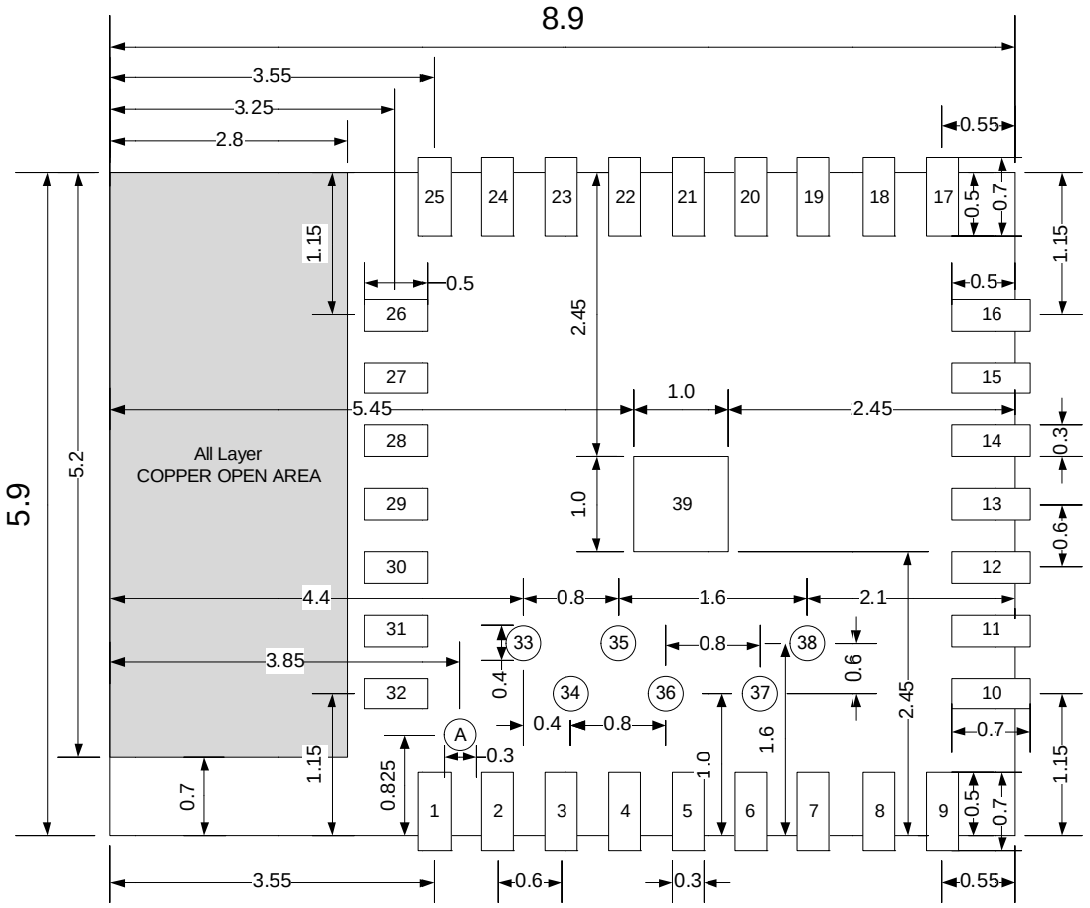
33,34,35,36,37,38 PAD : 0.4Ø

- Top View (Bottom pad)

<Figure 4. Physical dimension>

5. Layout

UNIT : mm



A : No1 Mark.(0.3Ø GND)

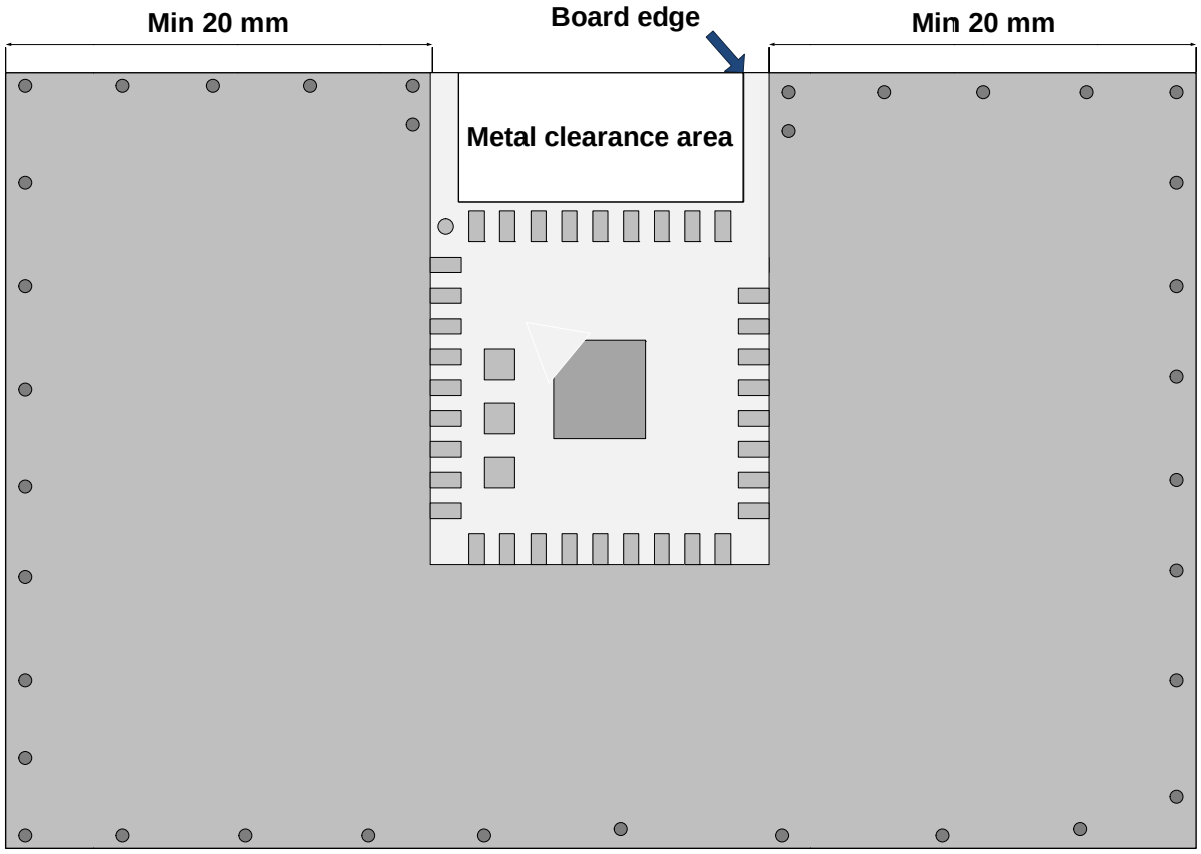
33,34,35,36,37,38 PAD : 0.4Ø

- Top View (Bottom pad)

<Figure 5. Layout>

5.1 Layout Guide

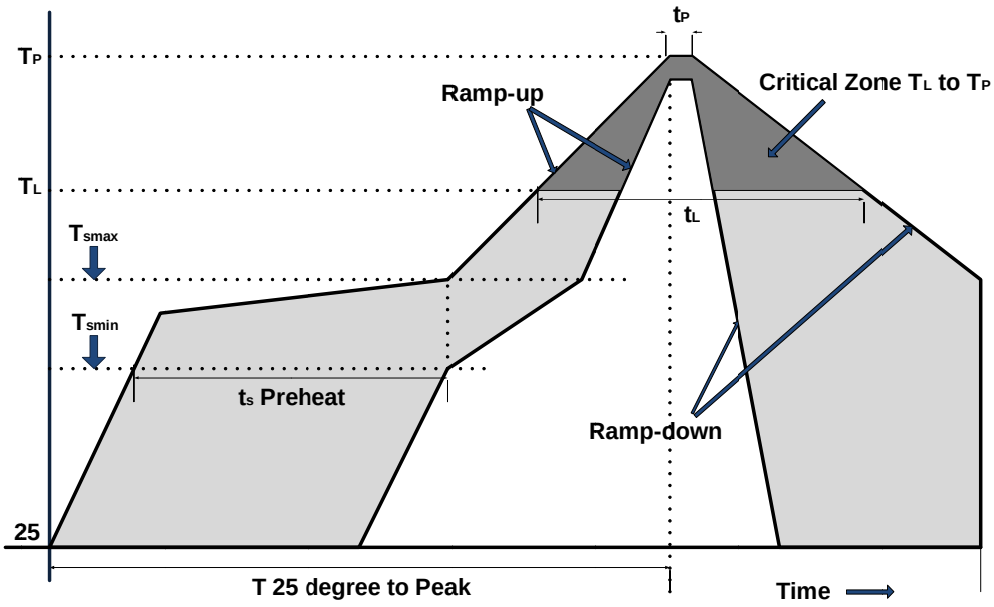
To achieve best radio performance for UTO-NBL-52A, it is recommended to use the module at the edge of the PCB as shown in Figure 6. Do not place any metal (traces, components, etc.) within the clearance area of the antenna. Connect all the GND pins directly to a solid GND plane. Place the GND vias as close to the GND pins as possible. Do not place plastic or any other dielectric material in touch with the antenna.



<Figure 6. Recommended layout>

6. Re-flow Temperature time profile

The data here is given only for guidance on solder and has to be adapted to your process and other re-flow parameters for example the used solder paste. The paste manufacturer provides a re-flow profile recommendation for his product.



<Figure 7. Soldering Temperature time profile>

Preheat		Main Heat		Peak	
Tsmax		TLmax		tpmax	
Temperature	Time	Temperature	Time	Temperature	Time
Degree	sec	Degree	sec	Degree	sec
150	100	217	90	260	10
		230	50		
Parameter				Value	Unit
Average ramp-up rate				3	Degree/sec
Average ramp-down rate				6	Degree/sec
Max. Time 25 degree to Peak Temperature				8	Min.

<Table 6 : Soldering temperature parameters>

Opposite side re-flow is prohibited due to module weight. Devices will withstand the

specified profile and will withstand up to 1 re-flows to a maximum temperature of 260 degree. The re-flow soldering profile may only be applied if the UTO-NBL-52A resides on the PCB side looking up. Heat above the solder eutectic point while the UTO-NBL-52A is mounted facing down may damage the module permanently.

7. Certification

7.1 Bluetooth SIG Listing

- Declaration ID : D038906 (End Product)

7.2 FCC

- FCC Identifier : 2AMD4UTO-NBL-52A

7.3 CE

- Certificate Number : KRLC12-1A

7.4 KC

- MSIP-CRM-uto-UTO-NBL-52

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